ABSTRACT OF THE DISCLOSURE

A differential input circuit comprising only low withstand voltage transistors, which reliability is not affected even if a high power supply voltage is used. The first and second clamp circuits input the differential input signals IN+ and IN- which vibrate between the ground potential and the power supply potential VDD, and output the signals INH+ and INH- of which the lower limit potential is the bias potential BIAS2, and the signals INL+ and INL- of which the upper limit potential is the bias potential BIAS3. Using these signals, the folded cascode amplification circuit generates the differential output signals OUT+ and OUT- which vibrate between the ground potential and the power supply potential VCC (VCC < VDD). The bias circuit generates the bias potential of the transistor inside the folded cascode amplification circuit. The gate potential of the transistor in the folded cascode amplification circuit is set such that the voltages between the gate and the source and between the gate and the drain are smaller than VCC.